	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1	"20050268019"	US-PGPUB; USPAT	2007/05/09 11:49
2	BRS	L2	1	1 and (ttl differential)	US-PGPUB; USPAT	2007/05/09 11:51
3	BRS	L3	97	ttl with differential with (translator converter)	US-PGPUB; USPAT	2007/05/09 12:22
4	BRS	L4	84	3 and @ad<"20040601"	US-PGPUB; USPAT	2007/05/09 11:55
5	BRS	L5	1	ttl with differential with (translator converter) with noise	US-PGPUB; USPAT	2007/05/09 12:41
6	BRS	L6	9	ttl with differential with (camera settop stb)	US-PGPUB; USPAT	2007/05/09 12:22
7	BRS	L7	22521	ttl differential with (camera settop stb)	US-PGPUB; USPAT	2007/05/09 12:22
8	BRS	L8	1264	transistor with differential with (translator converter)	US-PGPUB; USPAT	2007/05/09 12:23
9	BRS	L9	0	transistor with differential with (translator converter) with (camera settop set-top stb)	US-PGPUB; USPAT	2007/05/09 12:24
10	BRS	L10	0	transistor with differential with (translator converter) same (camera settop set-top stb)	US-PGPUB; USPAT	2007/05/09 12:24
11	BRS	L12	7	ttl with differential with (translator converter) and (camera settop set-top stb)	US-PGPUB; USPAT	2007/05/09 12:25
12	BRS	L11	52	transistor with differential with (translator converter) and (camera settop set-top stb)	US-PGPUB; USPAT	2007/05/09 12:28
13	BRS	L13	31	ttl with differential with (translator converter) same (noise advantage better efficient)	US-PGPUB; USPAT	2007/05/09 12:42

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	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1	"20050268019"	US-PGPUB; USPAT	2007/05/09 14:42
2	BRS	L2	1	1 and running	US-PGPUB; USPAT	2007/05/09 14:45
3	BRS	L3	1	1 and (caching with external with condition)	US-PGPUB; USPAT	2007/05/09 15:12
4	BRS	L4	7178	(PHY LINK) with (FPGA translator converter)	US-PGPUB; USPAT	2007/05/09 15:12
5	BRS	L5	65	(PHY with LINK) with (FPGA translator converter)	US-PGPUB; USPAT	2007/05/09 15:12

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	267	fpga with interface with controller	USPAT	2007/05/09 16:40
2	BRS	L2	15	fpga with interface with controller with rom	USPAT	2007/05/09 16:27
3	BRS	L3	117	fpga with interface with controller with programmable	USPAT	2007/05/09 16:40
4	BRS	L4	1	fpga with interface with controller with programmable with interrupt	USPAT	2007/05/09 16:41
5	BRS	L5	64	(programmable with controller) with (PHY MAC (link adj1 layer))	USPAT	2007/05/09 16:42